REMARKS

Claims 1-67 are now pending in this application. Claim 10 is amended. Claims 68-110 have been canceled.

Claims 1-7, 11, 12, 17-21, 23, 24, 28-34, 37, 41-45, 47-53, 56, 57 and 62-66 stand rejected under 35 § U.S.C. 103(a) as being unpatentable over Ohsawa et al., "Memory design using a one-transistor gain cell on SOI" (IEEE 2002)("Ohsawa") in view of Pham et al. (U.S. Patent No. 6,838,322)("Pham"). The rejection is respectfully traversed.

Claim 1 recites a "memory device" and claim 32 recites a "processor system." Each of claims 1 and 32 further recites a "storage transistor comprising: a body portion between first and second source/drain regions" and "a gate structure, wherein the gate structure wraps at least partially around the body portion in at least two spatial planes."

Claim 23 recites a "dynamic random access memory (DRAM) cell" comprising, *inter alia*, a "storage transistor comprising: a body portion between first and second source/drain regions, the body portion containing a heavily doped region of a first conductivity type adjacent to the second source/drain region and separated from the first source/drain region" and "a gate structure, the gate structure wrapping at least partially around the body portion in at least two spatial planes."

Claim 28 recites a "memory array" comprising, *inter alia*, "a plurality of memory cells, each memory cell comprising a storage transistor . . ., the storage transistor comprising: . . . a plurality of gates at least partially surrounding the body portion."

Claim 30 recites a "semiconductor chip" comprising, *inter alia,* "a plurality of dynamic random access memory (DRAM) cells, at least one DRAM cell comprising a partially depleted storage transistor" and "a gate structure, the gate structure wrapping at least partially around each fin-shaped structure."

Claim 47 recites a "transistor device" comprising, *inter alia,* "a body portion for storing charge, . . . the body portion including a doped region of a second conductivity type adjacent to the second source/drain region and separated from the first source/drain region" and "a gate structure wrapping around the body portion in at least two spatial planes."

As agreed by the Office Action, Ohsawa does not teach or suggest a gate structure wrapping around a body portion or a plurality of gates. Ohsawa teaches memory based on a one-transistor gain cell. In order to accomplish Ohsawa's one-transistor gain cell, a planar MOSFET with an electrically floating body is used. Ohsawa at p. 1510, Section II. Pham, on the other hand, teaches a fabrication process for forming a FinFET.

Neither Pham nor Ohsawa makes any reference, mention, or suggestion that it is possible to use Pham's FinFET as a storage device. Applicant respectfully submits that this rejection is based improperly on hindsight.

It is understood by those skilled in the art that FinFETs provide very good gate control in the sub-threshold and linear regions. FinFETs allow use of an undoped channel and can be fully depleted devices. As mentioned in Pham, when planar devices are scaled, intense channel doping is needed. However, the channel doping degrades carrier mobility and junction characteristics. Pham at col. 1, lines 25-34. Also, the fabrication processes described by Pham do not include channel doping.

Pham has not suggested that the disclosed FinFET could be for use as a storage transistor. The claimed storage transistor uses a substantial floating body effect in its operation; Pham does not discuss how the described FinFET may be used as a storage device, or how the FinFET is in any other way suited for use in a memory cell. The constraints required for a conventional FinFET are very different from the constraints required for constructing a storage device. Applicants found that a FinFET could be used as a storage device by suitably doping source/drain regions, but the Office Action has not shown any motivation in the prior art at the time the invention was made where a FinFET or other structurally similar transistor is similarly employed as a storage device.

"The showing of motivation to combine must be clear and particular, and it must be supported by actual evidence." Teleflex, Inc. v. Ficosa North America Corp., 299 F.3d 1313, 1334 (Fed. Cir. 2002), citing In re Dembiczak, 175 F.3d at 999. "Broad, conclusory statements regarding the teaching of the multiple references, standing alone, are not 'evidence.'" In re Dembiczak, 175 F.3d at 999.

While the Office Action is correct that "any judgment on obvious is in a sense necessarily a reconstruction based upon hindsight, the Federal Circuit requires a "rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references." McGinley, 262 F.3d at 1351; In re Dembiczak, 175 F.3d at 999. This is required because "[t]he genius of invention is often a combination of known elements which in hindsight seems preordained. " McGinley, 262 F.3d at 1351; In re Dembiczak, 175 F.3d at 999.

This "rigorous application" is "the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis." In re Dembiczak, 175

F.3d at 999; "To prevent hindsight invalidation of patent claims, the law requires some teaching, suggestion or reason to combine cited references." McGinley, 262 F.3d at 1351. "When the art in question is relatively simple . . . the opportunity to judge by hindsight is particularly tempting. Consequently, the tests of whether to combine references need to be applied rigorously." Id.

At the same time, "as a 'useful general rule,' . . . references that teach away [from a particular combination] cannot serve to create a prima facie case of obviousness." McGinley, 262 F.3d at 1353-4, citing In re Gurley, 27 F.3d 551, 553 (Fed. Cir. 1994). The Federal Circuit has also held that a modification that produces a "seemingly inoperable device" necessarily teaches away from that modification. McGinley, 262 F.3d at 1354, citing In re Sponnoble, 405 F.2d 578, 587 (CCPA 1969); In re Gordon, 733 F.2d 900 , 902 (Fed. Cir. 1984).

The Office Action does not attempt any explanation of how one of ordinary skill, having no access to Applicant's disclosure, would modify a conventional FinFET, as described by Pham, for use as a storage transistor such as the transistor described by Ohsawa. The Office Action can only point to a passing statement in Pham that states that the invention is not limited to the described embodiments; this is no substitute for a concrete teaching, motivation or suggestion necessary to use the described FinFET in a memory embodiment and such that it operates in a completely different way from that disclosed in Pham, requiring numerous untaught modifications of Phan. Pham teaches away from Applicant's invention by, and to combine the FinFET of Pham with Ohsawa would create a "seemingly inoperable device."

For at least these reasons withdrawal of this rejection is respectfully requested.

Claims 8 and 35 stand rejected under § 103(a) as being unpatentable over Ohsawa in view of Pham, as applied to claim 1, and further in view of Hu et al. (U.S. Patent No. 5,448,513)("Hu"). The rejection is respectfully traversed.

Claims 8 and 35 depend from claims 1 and 32. As discussed above, one of ordinary skill in the art would not have been motivated to combine Ohsawa and Pham as suggested by the Examiner. Likewise, Hu does not provide and teaching, suggestion or motivation for the proposed combination. Therefore, for at least these reasons, withdrawal of this rejection is respectfully requested.

Claims 14-16, 38-40, and 59-61 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohsawa in view of Pham, as applied to claim 1, and further in view of Matsumoto et al. (U.S. Patent No. 6,806,537)("Matsumoto"). The rejection is respectfully traversed.

As discussed above, one of ordinary skill in the art would not have been motivated to combine Ohsawa and Pham as suggested by the Examiner. Likewise, Matsumoto does not provide and teaching, suggestion or motivation for the proposed combination. For at least these reasons, Applicant respectfully requests the withdrawal of this rejection.

Claims 15 and 58 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohsawa in view of Pham, as applied to claim 1, and further in view of Takasu (U.S. Patent No. 5,307,305). The rejection is respectfully traversed.

As discussed above, one of ordinary skill in the art would not have been motivated to combine Ohsawa and Pham as suggested by the Examiner. Likewise, Takasu does not provide and teaching, suggestion or motivation for the proposed combination. For at least these reasons, Applicant respectfully requests the withdrawal of this rejection.

Claims 9, 10, 27, 36, 54, and 55 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohsawa in view of Pham, as applied to claim 1, and further in view of Yu et al. (U.S. Patent No. 6,221,724)("Yu"). The rejection is respectfully traversed.

As discussed above, one of ordinary skill in the art would not have been motivated to combine Ohsawa and Pham as suggested by the Examiner. Likewise, Yu does not provide and teaching, suggestion or motivation for the proposed combination. For at least these reasons, Applicant respectfully requests the withdrawal of this rejection.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Dated: October 5, 2005

Respectfully submitted,

By____________________
Thomas J. D'Amico
Registration No.: 28,371
Jerome Deluca
Registration No.: 55,106
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant